

What is claimed is:

1. A semiconductor integrated circuit device comprising:

5 a high-threshold N-channel type MIS field effect transistor connected between a real high-potential power supply line and a pseudo high-potential power supply line; and

10 a load circuit having a low-threshold P-channel type MIS field effect transistor and a low-threshold N-channel type MIS field effect transistor, wherein:

15 a first power supply terminal of said load circuit is connected to said pseudo high-potential power supply line, and a second power supply terminal of said load circuit is connected to a real low-potential power supply line.

20 2. The semiconductor integrated circuit device as claimed in claim 1, wherein a back gate of said low-threshold P-channel type MIS field effect transistor is connected to said pseudo high-potential power supply line, and a back gate of said low-threshold N-channel type MIS field effect transistor is connected to said real low-potential power supply line.

25 3. The semiconductor integrated circuit device as claimed in claim 1, further comprising:

30 a waveshaping circuit which receives a control signal for controlling said high-threshold N-channel type MIS field effect transistor, and performs waveshaping so that said control signal rises slowly, and wherein:

an output signal of said waveshaping circuit is supplied to a gate of said high-threshold N-channel type MIS field effect transistor.

35 4. The semiconductor integrated circuit device as claimed in claim 3, wherein said high-threshold N-channel type MIS field effect transistor is configured as a source follower, and a voltage on said pseudo high-

potential power supply line connected to the source of said high-threshold N-channel type MIS field effect transistor rises slowly in response to the slowly rising output signal of said waveshaping circuit supplied to  
5 said gate.

5. The semiconductor integrated circuit device as claimed in claim 3, wherein said waveshaping circuit comprises a high-threshold final-stage MIS field effect transistor having a large gate length and a small gate  
10 width, or a plurality of high-threshold final-stage MIS field effect transistors connected in series.

6. The semiconductor integrated circuit device as claimed in claim 3, wherein said waveshaping circuit comprises a digital/analog converter.

15 7. The semiconductor integrated circuit device as claimed in claim 6, wherein said load circuit comprises a memory circuit, and said digital/analog converter outputs a voltage that is lower than a normal operating voltage of said memory and that only guarantees the retention of  
20 stored contents, thereby achieving a reduction in backup standby power consumption.

8. A semiconductor integrated circuit device comprising:

25 a high-threshold N-channel type MIS field effect transistor connected between a real high-potential power supply line and a pseudo high-potential power supply line, said high-threshold N-channel type MIS field effect transistor being controlled by receiving a slowly rising control signal to a gate thereof; and

30 a load circuit having a low-threshold P-channel type MIS field effect transistor and a low-threshold N-channel type MIS field effect transistor, wherein:

35 a first power supply terminal of said load circuit is connected to said pseudo high-potential power supply line, and a second power supply terminal of said load circuit is connected to a real low-potential

power supply line.

9. A semiconductor integrated circuit device comprising:

5 a high-threshold MIS field effect transistor of a first conductivity type, connected between a first real power supply line and a first pseudo power supply line;

10 a load circuit having a low-threshold MIS field effect transistor of said first conductivity type and a low-threshold MIS field effect transistor of a second conductivity type; and

15 a level conversion circuit which receives a control signal of a first level for controlling said high-threshold MIS field effect transistor of said first conductivity type, and which converts said control signal of said first level into a control signal of a second level and supplies said control signal of said second level to a gate of said high-threshold MIS field effect transistor of said first conductivity type, wherein:

20 a first power supply terminal of said load circuit is connected to said first pseudo power supply line, and a second power supply terminal of said load circuit is connected to a second real power supply line.

25 10. The semiconductor integrated circuit device as claimed in claim 9, wherein said high-threshold MIS field effect transistor of said first conductivity type and said level conversion circuit are together constructed as a module.

30 11. The semiconductor integrated circuit device as claimed in claim 9, wherein said first level is equal to a signal interface level of said load circuit, and said second level is a level greater than said first level.

35 12. The semiconductor integrated circuit device as claimed in claim 9, wherein said first real power supply line is a real high-potential power supply line, said second real power supply line is a real low-potential

power supply line, said first pseudo power supply line is a pseudo high-potential power supply line, and said high-threshold MIS field effect transistor of said first conductivity type is a high-threshold N-channel type MIS field effect transistor, wherein:

5 a drain of said high-threshold N-channel type MIS field effect transistor is connected to said real high-potential power supply line, a source thereof is connected to said pseudo high-potential power supply line, and a back gate thereof is connected to said real low-potential power supply line.

10 13. The semiconductor integrated circuit device as claimed in claim 9, wherein said first real power supply line is a real high-potential power supply line, said second real power supply line is a real low-potential power supply line, said first pseudo power supply line is a pseudo high-potential power supply line, and said high-threshold MIS field effect transistor of said first conductivity type is a high-threshold P-channel type MIS field effect transistor, wherein:

20 a source and back gate of said high-threshold P-channel type MIS field effect transistor are connected to said real high-potential power supply line, and a drain thereof is connected to said pseudo high-potential power supply line.

25 14. The semiconductor integrated circuit device as claimed in claim 9, further comprising:

30 a waveshaping circuit which receives the output signal of said level conversion circuit, and performs waveshaping so that the output signal of said level conversion circuit rises slowly, and wherein:

an output signal of said waveshaping circuit is supplied to a gate of said high-threshold MIS field effect transistor of said first conductivity type.

35 15. The semiconductor integrated circuit device as claimed in claim 14, wherein said high-threshold MIS field effect transistor of said first conductivity type

is configured as a source follower, and a voltage on said first pseudo power supply line connected to the source of said high-threshold MIS field effect transistor of said first conductivity type rises slowly in response to the slowly rising output signal of said waveshaping circuit supplied to said gate.

16. The semiconductor integrated circuit device as claimed in claim 9, wherein a physical shield is provided over a signal wiring line from said level conversion circuit to said high-threshold MIS field effect transistor of said first conductivity type.

17. The semiconductor integrated circuit device as claimed in claim 16, wherein said semiconductor integrated circuit device has a multilayered wiring structure, and said shield is formed in a prescribed intermediate wiring layer, while a signal line of a signal interface level of said load circuit is formed in a wiring layer located above said prescribed intermediate wiring layer.

18. The semiconductor integrated circuit device as claimed in claim 14, wherein said waveshaping circuit comprises a high-threshold final-stage MIS field effect transistor having a large gate length and a small gate width, or a plurality of high-threshold final-stage MIS field effect transistors connected in series.

19. The semiconductor integrated circuit device as claimed in claim 14, wherein said waveshaping circuit comprises a digital/analog converter.

20. The semiconductor integrated circuit device as claimed in claim 19, wherein said load circuit comprises a memory circuit, and said digital/analog converter outputs a voltage that is lower than a normal operating voltage of said memory and that only guarantees the retention of stored contents, thereby achieving a reduction in backup standby power consumption.

21. A semiconductor integrated circuit device comprising:

a high-threshold MIS field effect transistor of a first conductivity type, connected between a first real power supply line and a first pseudo power supply line; and

5 a load circuit having a low-threshold MIS field effect transistor of said first conductivity type and a low-threshold MIS field effect transistor of a second conductivity type, wherein:

10 a first power supply terminal of said load circuit is connected to said first pseudo power supply line, and a second power supply terminal of said load circuit is connected to a second real power supply line, wherein said first pseudo power supply line is brought outside a chip.

15 22. A semiconductor integrated circuit device comprising:

a high-threshold MIS field effect transistor of a first conductivity type, connected between a first real power supply line and a first pseudo power supply line; and

20 a load circuit having a low-threshold MIS field effect transistor of said first conductivity type and a low-threshold MIS field effect transistor of a second conductivity type, wherein:

25 a first power supply terminal of said load circuit is connected to said first pseudo power supply line, and a second power supply terminal of said load circuit is connected to a second real power supply line, wherein said first real power supply line is brought outside a chip.

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